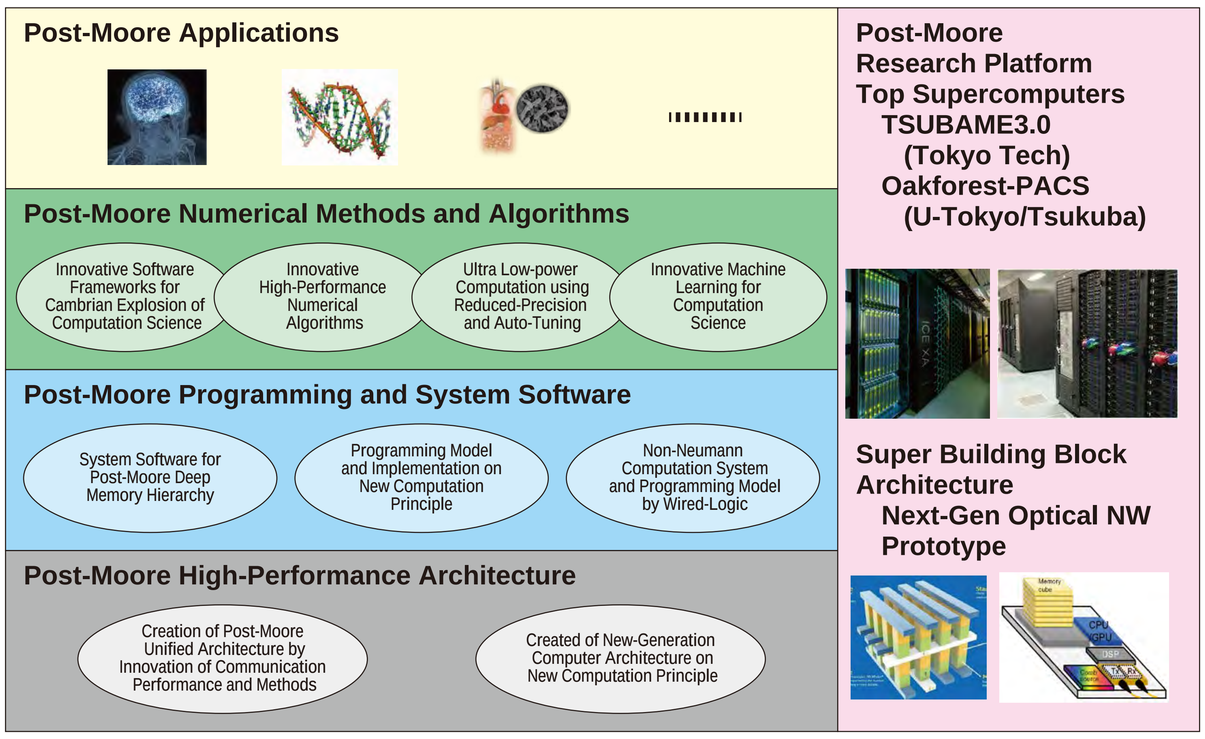
Challenges towards Cambrian Explosion in the Post-Moore Era

Project Overview

Slowdown and inevitable end in exponential scaling of processor performance, the end of Moore's Law is predicted to occur around 2025-2030. The system FLOPS will cease to improve, resulting in serious consequences for IT, especially supercomputing.

We claim that data-oriented parameters, such as bandwidth and capacity, or BYTES, are the new parameters that will allow continuous improvement even after computing performance or FLOPS ceases to improve. This will lead to so-called Cambrian explosion in computer architecture and algorithms including the new computational principles.

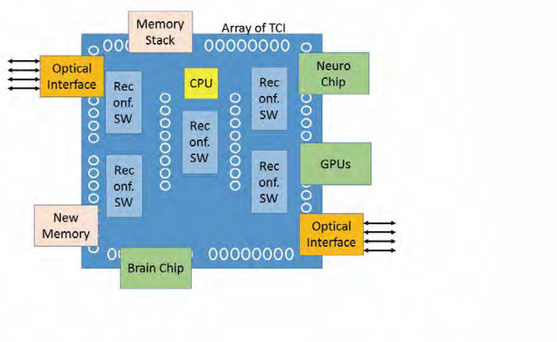
Such transition from FLOPS to BYTES will lead to disruptive changes in the overall systems from applications, algorithms, software to architecture.



Architecture

Unified Architecture:

In the Post-Moore era, processor chips, memory, NW will not be implemented on a single technology. The key technology is for a methodology to integrate various heterogeneous device into a system.



Next-Gen Architecture based on New Principle:

For IT infrastructures in extreme big-data era, novel device architectures including 3D-stacked devices, non-volatile devices, nano-photonics devices. New computational principle is required to exploit them to compose new architecture in the post-Moore era.

Programming & System Software

Exploiting Deeper Memory Hierarchy:

System software should be exploit deeper memory hierarchy including heterogeneous types of memory. Topics include scheduling such memory hierarchy, fault tolerance with NVM.

Programming Model on New Principle:

Design and implementation of novel programming model are required to on support new computation principle with extremely high BW memory and network.

Towards non von Neumann system:

To support improvement of BW metrics, computation system and compilers are required to support non von Neumann model. Support for customizable logic will be included.

Numerical Methods & Algorithms

Framework to Support Cambrian Explosion in Architecture:

Framework for software algorithm will be reconsidered based on byte-centric metric focused in novel architectures in Cambrian explosion.

Innovative Numerical Algorithms:

Numerical algorithms should be restructured to support new architectures, including dense matrices, iterative stencils, eigen/singular value solver, etc.

Ultra Low Power using Reduced Precision:

In order to achieve ultra low power, trans-precision and approximate computing will be pursued, while securing precision of the solution. Auto-tuning techniques are applied.

Innovative Machine Learning for Computational Science:

Machine learning itself should be adapted to new explosively variant architecture. Also machine-learning based mathematical models are developed for high performance/precise simulations.

Post-Moore's Era Supercomputing (PMES17) Workshop

Co-located with SC17
Nov 13, 2017
Co-Chaired by
Satoshi Matsuoka (Tokyo Tech)
Jeffrey S. Vetter (ORNL)

To explore the scientific issues, challenges, and opportunities for supercomputing beyond the scaling limits of Moore's Law

https://sites.google.com/view/pmes17/

Project Leader: Satoshi Matsuoka (Tokyo Tech)
Hideharu Amano (Keio Univ), Kengo Nakajima (Univ of Tokyo), Koji Inoue (Kyushu Univ), Kenjiro Taura (Univ of Tokyo), Kentaro Sano (Tohoku Univ), Takeshi Iwashita (Hokkaido Univ), Takahiro Katagiri (Nagoya Univ), Takashi Shimokawabe (Univ of Tokyo) Toshihiro Hanawa (Univ of Tokyo), Toshio Endo (Tokyo Tech)

S. Matsuoka et al. : From FLOPS to BYTES: Disruptive Change in High-Performance Computing towards the Post-Moore Era. ACM Computing Frontiers 2016, Invited paper.