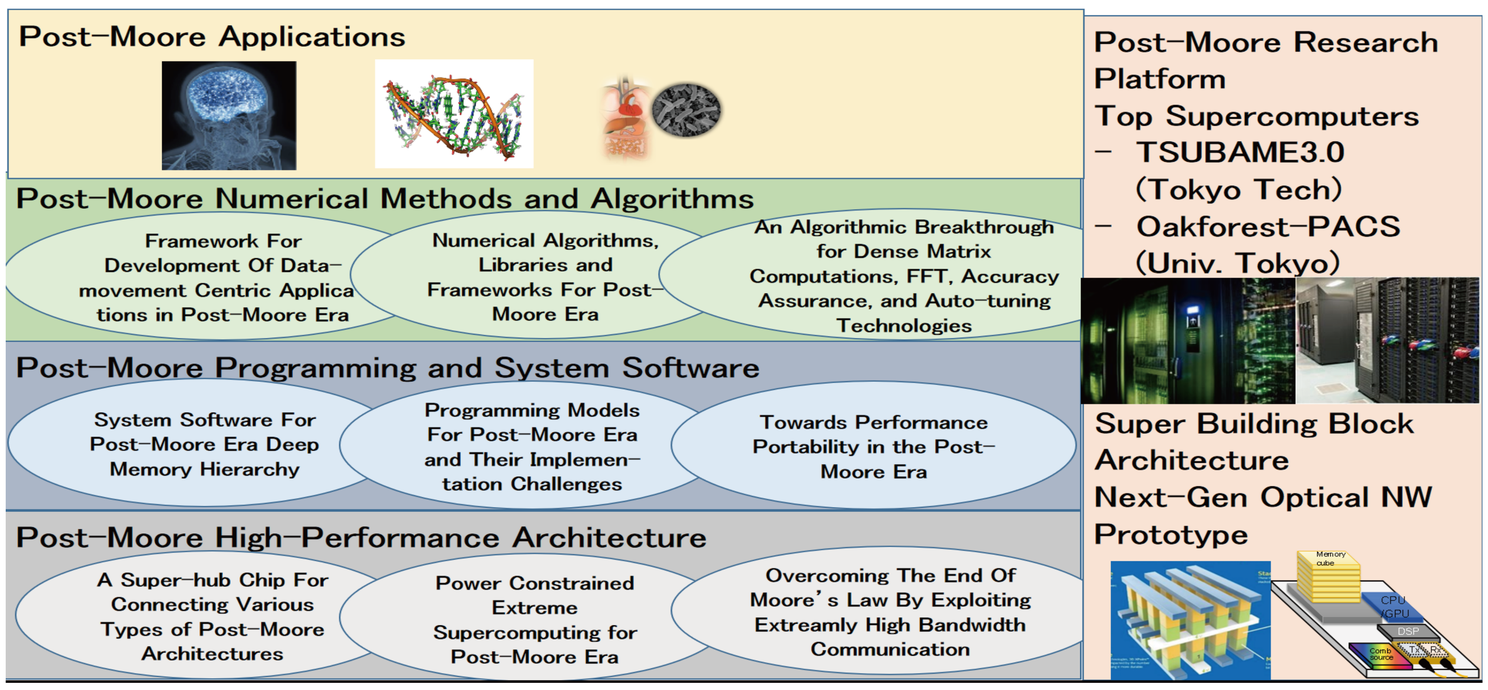
Research Challenges towards the Post-Moore Era

Project Overview

Slowdown and inevitable end in exponential scaling of processor performance, the end of Moore's Law is predicted to occur around 2025-2030. The system FLOPS will cease to improve, resulting in serious consequences for IT, especially supercomputing.

We claim that data-oriented parameters, such as bandwidth and capacity, or BYTES, are the new parameters that will allow continuous improvement even after computing performance or FLOPS ceases to improve. This is due to continued advances in storage device technologies and optics, and 3-D packaging technologies.

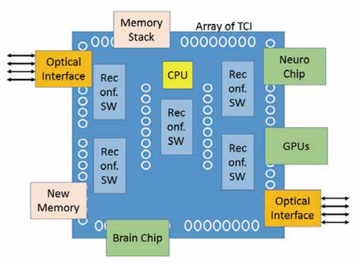
Such transition from FLOPS to BYTES will lead to disruptive changes in the overall systems from applications, algorithms, software to architecture, as to what parameter to optimize for.



Post-Moore High-Performance Architecture

Super-hub Chips

In the Post-Moore era, chips will not be implemented on a single technology. The key technology is for a methodology to integrate various heterogeneous device into a system.



Power Constrained Extereme SC

Power is the most critical concerns on supercomputing. The promising approaches are overprovisioned system design, reducing the amount of FLOPS, and the concept of approximate computing.

Exploiting Extreme BW Communication

As future HPC communication, the dense wavelength division multiplexing (WDWM) is promising. Reconsideration of systems will be done based on concept of wavelength bank.

Post-Moore Programming & System Software

Exploiting Deeper Memory Hierarchy

System software should be exploit deeper memory hierarchy including heterogeneous types of memory. Topics include scheduling such memory hierarchy, fault tolerance with NVM.

Towards Performance Portability

For performance portability in future, modeling and exploiting heterogeneous architecture including FPGA and various many-core architectures are required.

Programming models

Key progress in programming models will be a proliferation of global view of data and computation. Towards this, silicon photonics, optical circuits tightly coupled with processors should be exploited.

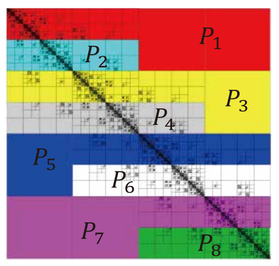
Post-Moore Numerical Methods & Algorithms

Framework for Data Centric Applications

Application framework will be made for the following components coupled with parallel-in- space/time (PiST) method: Nonlinear algorithm, AMR and coupler for muiltiphysics.

Numerical Algorithms

Algorithms should be reconsidered for BYTE centric architecture. For dense matrices, H-matrix approximation is promising with its lower F/B ratio.



Algorithmic Breakthrough

Algorithms for matrix computation and FFT should be modeled and redesigned for Post-moore architecture including FPGA. They are also coupled with new accuracy assurance and auto-tuning technologies.

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S. Matsuoka et al. : From FLOPS to BYTES: Disruptive Change in High-Performance Computing towards the Post-Moore Era. ACM Computing Frontiers 2016, Invited paper.

Post-Moore' s Era Supercomputing (PMES16) Workshop

Co-located with SC16
Nov 14, 2016
Co-Chaired by
Satoshi Matsuoka (Tokyo Tech)
Jeffrey S. Vetter (ORNL)

To explore the scientific issues, challenges, and opportunities for supercomputing beyond the scaling limits of Moore's Law
https://sites.google.com/site/2016pmes/